IN THE CLAIMS

1. (Currently Amended) A method comprising:

determining an optimum splitting variable for dividing a programmable logic array (PLA) into a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

dividing a set of equations representing a PLA into a first set of equations representing a first sub-PLA and a second set of equations representing a second sub-PLA based on the splitting variable;

determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA;

applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and

controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA.

2. (Original) The method of claim 1, wherein the PLA to be divided is partially optimized by computer aided design.

3. (Original) The method of claim 1, further comprising merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA.

Claims 4-5 (Canceled)

6. (Original) The method of claim 1, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

7. (Original) The method of claim 1, further comprising delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA.

8. (Original) The method of claim 1, wherein the step of determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA.

9. (Original) The method of claim 1, wherein determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design.

10. (Currently Amended) A method comprising:

determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

dividing the set of equations representing the PLA into equations representing the plurality of sub-PLAs;

merging outputs of the equations representing the plurality of sub-PLAs;

determining a topological circuit representation of the equations representing the plurality of sub-PLAs;

applying gating logic to the topological circuit representation of the plurality of sub-PLAs; and

controlling power consumption in the topological representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption,

wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

11. (Original) The method of claim 10, wherein the PLA to be divided is partially optimized by computer aided design.

12. (Original) The method of claim 10, wherein the equations representing the plurality of sub-PLAs are divided recursively based on a determined optimum splitting variable for each equation representing a sub-PLA.

13. (Original) The method of claim 12, wherein each product of the equations representing the plurality of sub-PLAs is obtained by omitting literals in the equations representing the PLA.

14. (Original) The method of claim 13, wherein a product of the omitted literals is used in the topological circuit representation of the plurality of sub-PLAs to gate a clock of each product of the plurality of sub-PLAs.

15. (Original) The method of claim 10, wherein the step of determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA; and

selecting a column with smallest overhead in the AND plane of the equations representing the PLA.

16. (Original) The method of claim 12, wherein the step of determining the optimum splitting variable for each of the equations representing the sub-PLA further comprises avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA.

17. (Currently Amended) A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determine a topological circuit representation of first sub-PLA and the second sub-PLA;

apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and

control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA.

18. (Original) The program storage device of claim 17, wherein the PLA to be divided is partially optimized by computer aided design.

19. (Original) The program storage device of claim 17, further comprising instructions that cause the machine to merge an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA,

wherein the instruction that causes the machine to merge the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA, forms a logical equivalent of the equations representing the PLA.

Claims 20-21 (Cancelled)

22. (Original) The program storage device of claim 17, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

23. (Original) The program storage device of claim 17, wherein the instructions that cause the machine to determine the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA.

24. (Currently Amended) A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA;

divide the set of equations representing the PLA into equations representing the plurality of sub-PLAs;

merge outputs of the equations representing the plurality of sub-PLAs;

determine a topological circuit representation of the equations representing the plurality of sub-PLAs;

apply gating logic to the topological circuit representation of the plurality of sub-PLAs; and

control power consumption in the topological circuit representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption,
wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.

25. (Original) The program storage device of claim 24, wherein the PLA to be divided is partially optimized by computer aided design.

26. (Original) The program storage device of claim 24, wherein the instruction causing the machine to divide the equations representing the plurality of sub-PLAs divides recursively based on a determined optimum splitting variable for each equation representing a sub-PLA.

27. (Original) The program storage device of claim 24, wherein the instruction causing the machine to determine the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the equations representing the PLA; and
selecting a column with smallest overhead in the AND plane of the equations representing the PLA.

28. (Original) The program storage device of claim 26, wherein the instruction causing the machine to determine the optimum splitting variable for each of the equations representing the sub-PLA further comprises avoiding unbalanced columns in an AND plane of the equations representing the sub-PLA; and selecting a column with smallest overhead in the AND plane of the equations representing the sub-PLA.

29. (Currently Amended) A method comprising:
determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, <u>said first sub-PLA and said</u>

second sub-PLA each having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

dividing the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA;

applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA.

30. (Previously Presented) The method of claim 29, wherein the PLA to be divided is partially optimized by computer aided design.

31. (Previously Presented) The method of claim 29, further comprising merging an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA, wherein merging the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA forms a logical equivalent of the PLA.

32. (Previously Presented) The method of claim 29, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

33. (Previously Presented) The method of claim 29, further comprising delaying a clock to an OR plane of one of the topological circuit representation of the first sub-PLA and the topological circuit representation of the second sub-PLA.

34. (Previously Presented) The method of claim 29, wherein the step of determining the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA.

35. (Previously Presented) The method of claim 29, wherein determining a topological circuit representation of first sub-PLA and the second sub-PLA is created by computer aided design.

36. (Currently Amended) A program storage device readable by a machine comprising instructions that cause the machine to:

determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA;

divide a set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable;

determine a topological circuit representation of the first sub-PLA and the second sub-PLA;

apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and

control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption,

wherein in the topological circuit representation an OR plane of the first sub-PLA is separated from an OR plane of the second sub-PLA.

37. (Previously Presented) The program storage device of claim 36, wherein the PLA to be divided is partially optimized by computer aided design.

38. (Previously Presented) The program storage device of claim 36, further comprising instructions that cause the machine to merge an output of the equations representing the first sub-PLA with an output of the equations representing the second sub-PLA,
wherein the instruction that causes the machine to merge the output of the equations representing the first sub-PLA with the equations representing the second sub-PLA, forms a logical equivalent of the equations representing the PLA.

39. (Previously Presented) The program storage device of claim 36, wherein the equations representing the first sub-PLA includes a plurality of products where the splitting variable is complemented and the equations representing the second sub-PLA includes a plurality of products where the splitting variable is uncomplemented.

40. (Previously Presented) The program storage device of claim 36, wherein the instructions that cause the machine to determine the optimum splitting variable further comprises avoiding unbalanced columns in an AND plane of the set of equations representing the PLA; and selecting a column with smallest overhead in the AND plane of the set of equations representing the PLA.